1 VME BIOS Settings

Photos of VME BIOS settings taken by Tobias Grussenmeyer on October $21^{st}\ 2014$

Phoenia	Phoenix - AwardBIOS CMOS Setup Utility Standard CMOS Features		
Date (nn:dd:yy) Tine (hh:nn:ss)	Tue, Oct 21 2014 20 : 14 : 13	Iten	
▶ IDE Channel Ø Master	[None]	Menu Level	
▶ IDE Channel Ø Slave	[None]	Change the i	
▶ IDE Channel 1 Master ▶ IDE Channel 1 Slave		year and cen	
Base Menory Extended Memory	640K		
Total Memory	2086912X 2087936X		

	AwardBIOS CMOS Set dvanced BIOS Feature	
► CPU Feature	[Press Enter]	Iten Help
▶ Hard Disk Boot Priority	[Press Enter]	1
CPU L1 & L2 Cache	[Enabled]	Menu Level ▶
Quick Power On Self Test	[Enabled]	
First Boot Device	[USB-FDD]	
Second Boot Device	[Hard Disk]	
Third Boot Device	[LAN]	
Boot Other Device	[Enabled]	
LAN-Boot ROM	[Endless]	
Boot Up NumLock Status	[On]	
Security Option APIC Mode	[Setup]	
MPIL MODE	[Enabled]	
MPS Version Control For O OS Select For DRAM > 64MB	S[1.4]	
HDD S.M.A.R.T. Capability	[Non-OS2]	
Full Screen LOGO Show	[Enabled]	
Summary Screen Show	[Disabled]	
Con one	[Disabled]	

Phoenix - AwardBIOS CMOS Setur Advanced Chipset Feature	
DRAM Timing Selectable [By SPD] x CAS Latency Time Auto	Item Help
x CHS Latency line Auto x DRAM RAS# to CAS# Delay Auto x DRAM RAS# Precharge Auto x Precharge delay (tRAS) Auto x System Memory Frequency Auto SLP_S4# Assertion Hidth [1 to 2 Sec.] System BIOS Cacheable [Enabled] Video BIOS Cacheable [Disabled] Memory Hole At 15M-16M [Disabled] PCI Express Root Port Func[Press Enter]	Menu Level >
** UDA Setting ** PEG/Onchip UGA Control [Auto] On-Chip Frame Buffer Size [8MB] DUMT Mode [DUMT] DUMT/FIXED Memory Size [224MB] Boot Display [CRT+EFP] ****:Move Enter:Select +/-/PH/PD:Halma E10.0	

	- AwardBIOS C 'nP/PCI Confi		Utilit	Y	
Init Display First Reset Configuration Data	[<mark>Onboard</mark>] [Disabled]		≜	Iter	Help
Resources Controlled By	[Auto(ESCD)]		Mer	u Level	۶
× IRQ Resources PCI/VGA Palette Snoop	Press Enter				
PCI Latency Timer(CLK) PCI Clock Line Size VME Memory Size	[32] [16] [1 GBute]				
Incoming UME SYSReset INT Pin 1 Assignment INT Pin 2 Assignment	[Enabled] [Auto] [Auto]				
INT Pin 3 Assignment INT Pin 4 Assignment INT Pin 5 Assignment	[Auto] [Auto]				
INT Pin 6 Assignment INT Pin 7 Assignment INT Pin 7 Assignment INT Pin 8 Assignment	[Auto] [Auto] [Auto]				
↑↓→←:Move Enter:Select +/-	[Auto] /PU/PD:Value : BIOS Default	F10:Save	ESC:Exi	t F1:Gene	eral Helj

Resources Controlled By IRO Resources	[Auto(ESCD)] Press Enter	▲ Iten Help
PCI/VGA Palette Snoop PCI Latency Timer(CLK) PCI Clock Line Size UME Memory Size Inconing UME SYSReset INT Pin 1 Assignment INT Pin 2 Assignment INT Pin 3 Assignment INT Pin 4 Assignment INT Pin 5 Assignment INT Pin 6 Assignment INT Pin 8 Assignment INT Pin 8 Assignment INT Pin 8 Assignment INT Pin 8 Assignment	[Disabled] [32] [16] [1 GByte] [Enabled] [Auto] [Auto] [Auto] [Auto] [Auto] [Auto] [Auto] [Auto] [Auto] [Auto]	Menu Level Set maximum TLP payload size for t PCI Express devices The unit is byte.
taximum Payload Size ↑↓→+:Move Enter:Select +	[128]	:Sau

