FPGA Pins		Signal Name	Connector Pins		
+	−		Conn.	+	−
P18	P17	LVDS_IN<0>	L	1	35
G16	F16	LVDS_IN<1>	L	2	36
C15	D15	LVDS_IN<2>	L	3	37
D18	C18	LVDS_IN<3>	L	4	38
D13	E13	LVDS_IN<4>	L	5	39
M14	N14	LVDS_IN<5>	L	6	40
H14	G13	LVDS_IN<6>	L	7	41
J16	H16	LVDS_IN<7>	L	8	42
D17	E17	LVDS_IN<8>	L	9	43
E15	F15	LVDS_IN<9>	L	10	44
J12	J11	LVDS_IN<10>	L	11	45
K14	L14	LVDS_IN<11>	L	12	46
K12	L11	LVDS_IN<12>	L	13	47
J13	K13	LVDS_IN<13>	L	14	48
M16	N15	LVDS_IN<14>	L	15	49
L17	M17	LVDS_IN<15>	L	16	50
B14	C14	LVDS_IN<16>	L	17	51
C13	D12	LVDS_IN<17>	L	18	52
B18	A19	LVDS_IN<18>	L	19	53
A17	B17	LVDS_IN<19>	L	20	54
H18	G18	LVDS_IN<20>	L	21	55
F17	G17	LVDS_IN<21>	L	22	56
K18	J18	LVDS_IN<22>	L	23	57
M18	N18	LVDS_IN<23>	L	24	58
M13	N13	LVDS_IN<24>	L	25	59
J15	K15	LVDS_IN<25>	L	26	60
G19	F19	LVDS_IN<26>	L	27	61
C19	B19	LVDS_IN<27>	L	28	62
L16	L15	LVDS_IN<28>	L	29	63
K17	J17	LVDS_IN<29>	L	30	64
N16	P16	LVDS_IN<30>	L	31	65
E19	E18	LVDS_IN<31>	L	32	66
		GND	L	33	67
		GND	L	34	68

FPGA Pins		Signal Name	Connector Pins		
+	−		Conn.	+	−
AJ21	AJ20	LVDS_OUT<0>	R	1	35
AL20	AL21	LVDS_OUT<1>	R	2	36
AJ17	AK17	LVDS_OUT<2>	R	3	37
AK20	AK19	LVDS_OUT<3>	R	4	38
AL19	AM19	LVDS_OUT<4>	R	5	39
AN16	AM16	LVDS_OUT<5>	R	6	40
AK15	AK14	LVDS_OUT<6>	R	7	41
AJ16	AJ15	LVDS_OUT<7>	R	8	42
AN20	AP20	LVDS_OUT<8>	R	9	43
AU21	AT21	LVDS_OUT<9>	R	10	44
AM17	AM18	LVDS_OUT<10>	R	11	45
AP21	AP22	LVDS_OUT<11>	R	12	46
AP16	AP17	LVDS_OUT<12>	R	13	47
AN18	AN19	LVDS_OUT<13>	R	14	48
AT22	AR22	LVDS_OUT<14>	R	15	49
AM21	AN21	LVDS_OUT<15>	R	16	50
AV23	AU22	LVDS_OUT<16>	R	17	51
AV18	AV19	LVDS_OUT<17>	R	18	52
AP18	AR19	LVDS_OUT<18>	R	19	53
AY18	AW18	LVDS_OUT<19>	R	20	54
AT20	AR20	LVDS_OUT<20>	R	21	55
AV21	AW21	LVDS_OUT<21>	R	22	56
BB18	BB19	LVDS_OUT<22>	R	23	57
AY20	BA20	LVDS_OUT<23>	R	24	58
BA19	AY19	LVDS_OUT<24>	R	25	59
BA22	BA21	LVDS_OUT<25>	R	26	60
AV20	AW20	LVDS_OUT<26>	R	27	61
AW22	AY22	LVDS_OUT<27>	R	28	62
BB24	BB23	LVDS_OUT<28>	R	29	63
AW23	AY23	LVDS_OUT<29>	R	30	64
BB22	BB21	LVDS_OUT<30>	R	31	65
AY24	BA24	LVDS_OUT<31>	R	32	66
		GND	R	33	67
		GND	R	34	68