Gandalf Specifications 0.1

- **From Analog Signal view:**

16 analog input channels,
Sampling performance 12 bit @ 0.5 Gsps or 14 bit @ 0.4 Gsps or

8 analog input channels (interleaved mode)
Sampling performance 12 bit @ 1 Gsps or 14 bit @ 0.8 Gsps

Analog input signal bandwidth 750 MHz (> max. Nyquist bandwidth @ 1Gsps)

Single ended dynamic ranges adjustable in 4V windows from
0V to -4V (lowest window) to
2V to -2V (highest window)

Programmable window offset by 16bit DAC (*AD5665RBCPZ-R2)* in a range of
-2V to 0V (30uV step size)

Analog input DC coupled. Single ended 50 Ohm analog input signal amplified by *LMH6552SD* to a differential signal to meet full dynamic range of the ADC

Analog digital conversion by *ADS5463* or *ADS5474*
12 bit 500 Msps pipelined ADCs, effective number of bits 10.5 or
14 bit 400 Msps pipelined ADCs, effective number of bits 11.2

SMC single ended input jacks

- **From Silicon Devices view:**

FPGA for data processing: *XC5VSX95T-2FFG1136C*
60k CLB Flip-Flops, 8Mbit Block RAM, 640 DSP Slices, speed grade -2
(500MHz Performance)

Functions:
Data collection and processing from 16 ADCs
Time and amplitude extraction (DSP filter)
Data concentration
Experiment trigger assignment
RPD trigger definition and creation
VME64x Interface
SLINK Interface
Aurora Interface
High frequency clocks control
System Monitoring (FPGA voltage and temperature)

Collects general purpose data from AMCs via I2C (DAC values, temperatures, AMC S/N, sampling mode)

FPGA for Data buffering: *XC5VLX30T-2FFG665C*

20K CLB Flip-Flops, 1,2Mbit Block RAM, 32 DSP Slices, speed grade -2 (500MHz Performance),

Functions:

Provides CACHE 144Mbit Memory by two QDRII+ devices (*CY7C1515AV18-250BZC*, 74Mbit dual port, double data rate memory, 36 bit per port),
Provides 8Gbit output buffer by two DDR2 devices (*HYB18T2G802BF-3S*, 4Gbit double data rate memory, 8 bit per port),
SLINK interface
Aurora Interface
System Monitoring (FPGA voltage and temperature)

CPLD for configuration and interface control: *XC2C512-7FGG324C*

Functions:

Handles VME64x interface
FPGA configuration with System ACE
Serial configuration and JTAG
USB interface
Board identification
Low frequency clocks
Power supply monitoring of all power rails

- **From Interface view:**

Modular experiment Clock and Trigger Interface:

Option 1a: TCS Gimli Card with opt. Receiver, connects via OC-3 fiber to the COMPASS Trigger Control System
Option 1b: TCS Gimli Card, connects via LEMO jack to the COMPASS Trigger Control System
Option 2: High precision Clock Gimli Card, with optional separate clock and trigger input via LEMO jacks.

Full VME64x interface (64 bit @ 10 MHz), block write and read geographic addressing

VXS interface to central trigger switch:

16 differential lanes (LVDS, 100 Ohm diff termination) per payload board (GANDALF) can be used in

Interleaved mode: 8 bit trigger time signaling, 8 bit signal amplitude transfer or
Normal mode: 16 bit trigger and amplitude channels combined (16 analog channel mode)
Additional I2C interface between all payload boards and trigger switch

USB Interface *CY7C68001-56LFXC:*
USB 2.0 Full and High Speed Interface Device for USB Peripheral (480 Mbit).
Programmable by local EEPROM or by adapted PC via Endpoint 0.
Connects to PC via a MiniUSB (AB) plug.

S-LINK Interface:
Both FPGAs are capable to communicate with the SLINK interface (32bits @ 40MHz)

Aurora Interface:
Chip to Chip Gigabit Interface.
16 lanes between the two FPGAs (8 lanes rx, 8 lanes tx)
Each lane has up to 3.125 Gbit performance

All other configuration ports (HF and LF clocks, Power Sequencer) are interconnected by I2C protocol.

Agilent Softouchprobe 64 bit debugging interface.

- **From Configuration view:**

Configuration of the FPGAs by
JTAG cable (serial)
System ACE CF card (serial, allows different configurations, partial configuration modes loaded from the CF)
VME interface (serial and parallel).

Maximum configuration performance: VME64x block write (64 bit @ 10 MHz) and Xilinx SelectMap Bus configuration (8bit @ 80MHz).

- **From Test and debugging view:**

Full Xilinx Fallback solution implemented:
Allows to copy actual FPGA configuration and last state of all Flip-Flops before/at a fault situation to CF
Up to 8 GB memory (CF) for dump of debugging data.

Additional JTAG chain for the QDRII+ devices (JTAG test only)